**PCIE test**

Revision history

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2017-09-13 | Initial | jiajiezhang |
| 0.2 | 2017-09-28 | Testcase 3.2.1-3, 3.2.5-11 dont need | jiajiezhang |
|  |  |  |  |

# ATE Verilog Test Bench Overview

Synopsys has solved the analog test issue for the PCIe 2 PHY by adding test features inside the IP and developing software that turns the analog testing portion of the IP into a pseudo digital scan. For analog testing, vectors are scanned in and scanned out of a JTAG port, similar to a digital scan. No complicated test code or analog test resources are required. Analog testing is a simple pass/fail operation.

## Methodology

All that is needed on a load board is a simple AC-coupled serial loopback for the PCIe 2 PHY, a reference clock, and a 200-Ω resistor. Typically, each test is configured through the JTAG port by writing to internal IP registers. A measurement is then made and compared against limits, and a pass/fail value is returned through the JTAG port.

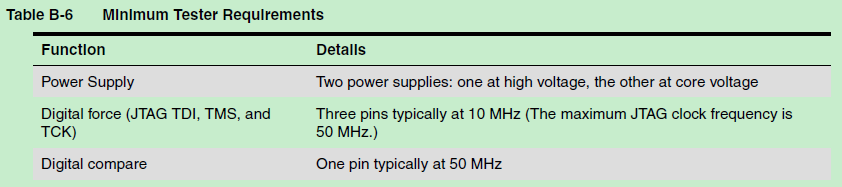
## Example Test

The TX\_DC\_LEVELS test is a good example to illustrate features inside the PCIe 2 PHY IP in use. In this test, the pattern generator is set up to send an “all 1’s” pattern. The transmit positive value is then placed on the test bus and measured with the ADC. This measurement is averaged and stored in the ALU. The transmit negative value is measured and then subtracted from the positive value. The resultant value is compared against limits that were placed in the ALU during the setup phase. A pass/fail result is then returned to the tester to complete the test. The following figure shows an example of the TX\_DC\_LEVELS test setup.

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# ATE Testing Details

## Tester Requirements



## Load Board Requirements

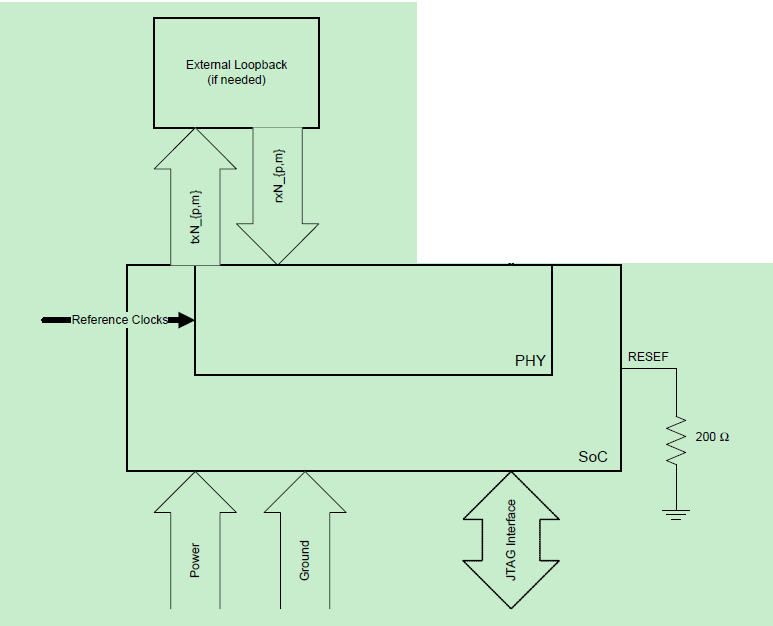
The PCIe 2 PHY requires an external 200-Ω resistor on the resref pin. To take advantage of the built-in test capabilities, an external AC-coupled loopback between the PCIe 2 PHY’s transmit and receive pins is required. If continuity/leakage measurements are required on the serial interface, place an optional relay on the signal path. To minimize any discontinuities in the signal path, take care when placing the relay. If only a continuity check is required, you can place a high-value resistor on the loopback path. The following figure shows the recommended layout.

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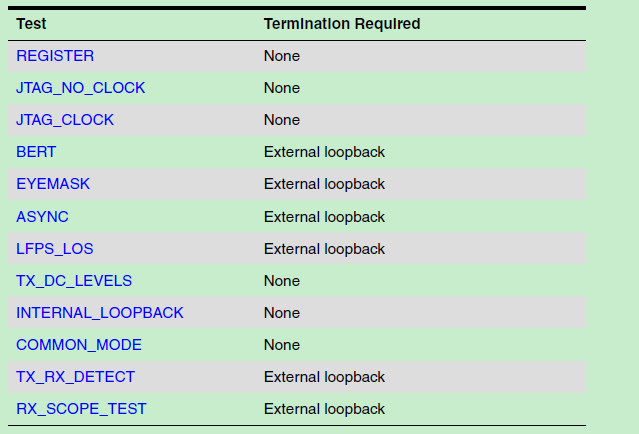
The horizontal lines are TX{p,m}. The vertical lines go to a probe point or connector to enable an ATE tester to perform a continuity test. The typical value for a high-value resistor is above 10 kΩ.

## Test Mode Pin Requirements

The following figure shows the external board requirements to place the PCIe 2 PHY in test mode.

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The following table lists the termination requirements for various tests.



## PAD list

|  |  |
| --- | --- |
| Ball name | Signal name |
| SPI\_MS3\_DI | SPI\_DBG\_DI |
| SPI\_MS3\_DO | SPI\_DBG\_DO |
| SPI\_MS3\_SCLK | SPI\_DBG\_SCLK |
| SPI\_MS3\_CS0N | SPI\_DBG\_CSN |
| SPI\_M2\_DI | TEST\_JTAG\_TDI |
| SPI\_M2\_DO | TEST\_JTAG\_TDO |
| SPI\_M2\_SCLK | TEST\_JTAG\_TCK |
| SPI\_M2\_CS0N | TEST\_JTAG\_TMS |
| PCIE\_RESREF | PCIE\_RESREF |
| PCIE\_RX0\_M | PCIE\_RX0\_M |
| PCIE\_RX0\_P | PCIE\_RX0\_P |
| PCIE\_TX0\_M | PCIE\_TX0\_M |
| PCIE\_TX0\_P | PCIE\_TX0\_P |
| PCIE\_RX1\_M | PCIE\_RX1\_M |
| PCIE\_RX1\_P | PCIE\_RX1\_P |
| PCIE\_TX1\_M | PCIE\_TX1\_M |
| PCIE\_TX1\_P | PCIE\_TX1\_P |

# ATE Tests

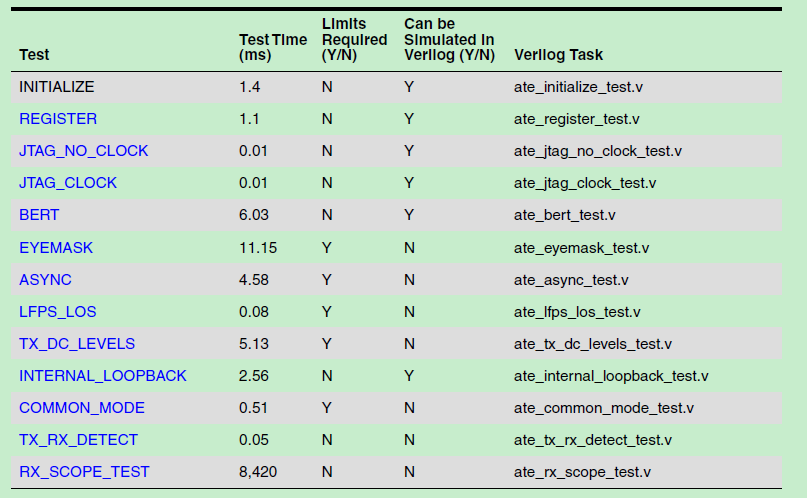
## Timing

Timing for sampling and comparing TDO occurs before the rising edge of the TCK. The following figure shows timing with a 16.6-MHz clock as TCK. Users must ensure that the TDO comparison with the expected TDO (as provided in the ate.vec file) occurs a quarter period after the falling edge of jtag\_tck, which ensures that TDO is stable at that point.

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## ATE Test Suite

The following table lists the ATE tests and their test times (assuming a 16.6-MHz JTAG clock frequency). Tests that require limits to be set are also indicated.

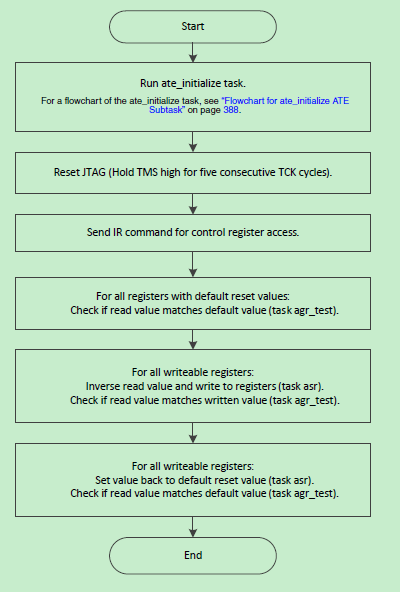


### ~~REGISTER~~

This test reads the default value of all readable registers in the PHY, then writes the inverse pattern and verifies the result. Finally, the test writes the default value back to the registers and verifies the result.

**External Loopback Required**: N

**Wafer Sort:** Y

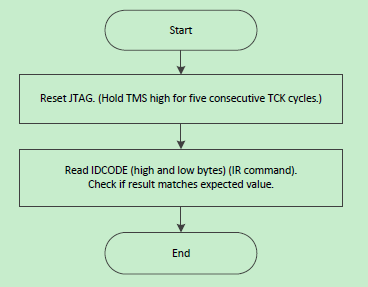


### ~~JTAG\_NO\_CLOCK~~

**External Loopback Required**: N

**Wafer Sort:** Y

This test verifies basic functions of the JTAG state machine by sending an IR IDCODE command and reading the IDCODE. This test requires only that the power to the PHY is present. This test does not provide much test coverage, but it verifies that the PHY can be accessed through the JTAG port. This is a good ‘first test’ to rule out connection issues from the tester to the PHY.

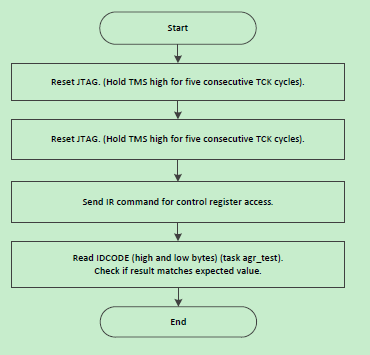


### ~~JTAG\_CLOCK~~

**External Loopback Required**: N

**Wafer Sort:** Y

This test is similar to the JTAG\_NO\_CLOCK test, but JTAG\_CLOCK reads the JTAG ID value from registers in the PCIe 2 PHY. To read registers in the PCIe 2 PHY, a reference clock must be present, and the PCIe 2 PHY must be enabled. After running JTAG\_NO\_CLOCK, JTAG\_CLOCK is a good second test to run to verify that both the reference clock is present and the PCIe 2 PHY is enabled.



### BERT

**External Loopback Required**: Y

**Wafer Sort**: N

It is highly recommended that you include this test, because it exercises the entire datapath. The BERT test checks the following in the PCIe 2 PHY:

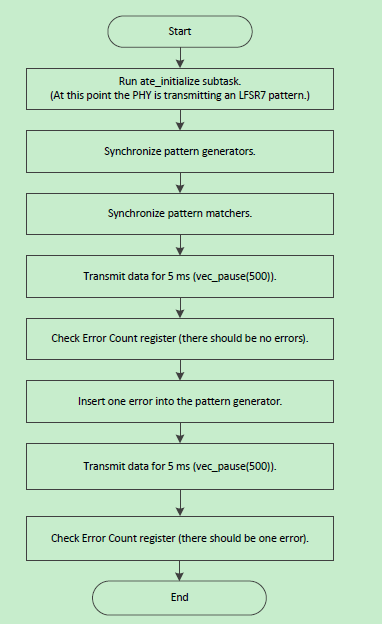
■ Signal path

■ Pattern matchers

■ Pattern generators

■ Error counters to be used in subsequent tests

This test uses an external loopback. A known LFSR7 pattern (default) is transmitted and matched at the receiver to verify that data can be passed from the transmitter to the receiver.

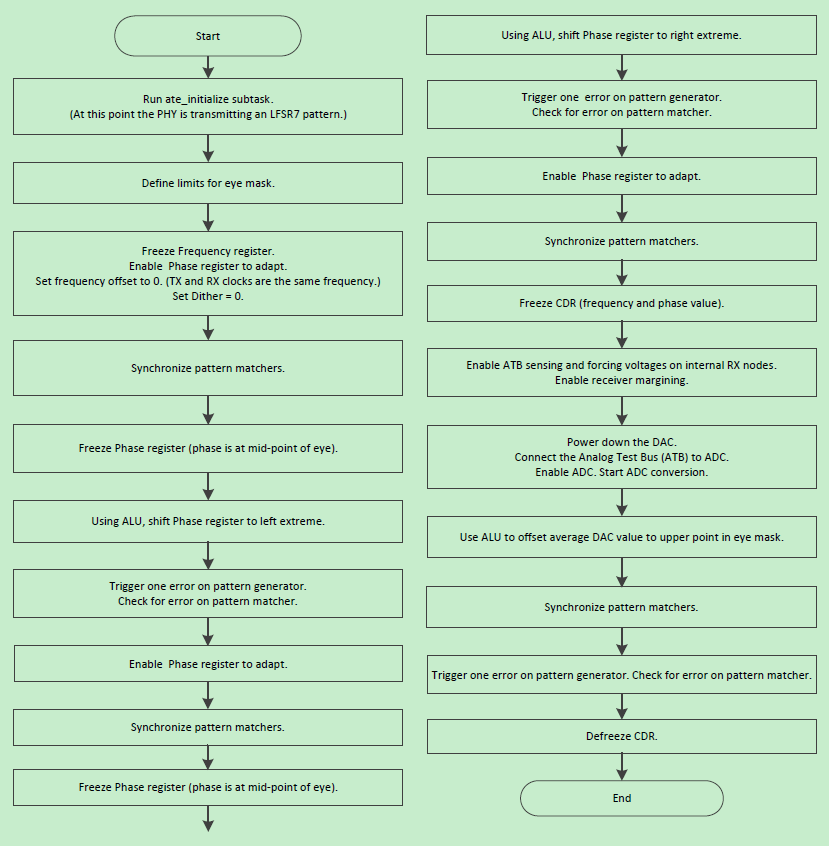


### ~~EYEMASK~~

**External Loopback Required**: Y

**Wafer Sort:** N

This test relies on the load board to have the channel loopbacked to itself. The external loopback trace should be a representative trace that the PCIe 2 PHY encounters in normal operation. The EYEMASK test enables users to define a diamond-shaped mask for template testing on the PCIe 2 PHY. The EYEMASK test is accomplished in the PCIe 2 PHY by moving the data strobe point in both voltage and phase at the receiver. Similar to the BERT test, the pattern generator creates a known pattern, which the pattern matcher matches. However, instead of sampling in the center of the eye, the strobe points used are the offset defined by the mask. The EYEMASK test enables users to test beyond a normal loopback test, in which the bit error rate is not guaranteed

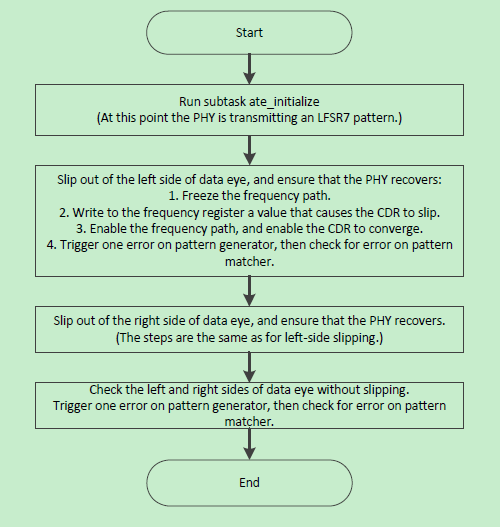


### ~~ASYNC~~

**External Loopback Required**: Y

**Wafer Sort:** N

This test checks the PCIe 2 PHY receiver. In most transceiver ATE testing, all tests are done in a synchronous environment. In the past, external equipment was required to perform any type of asynchronous testing. This requirement usually involved having some type of relay matrix to MUX the external signal to all the channels. This setup takes time to implement and requires a device be tested on a tester with such equipment. The PCIe 2 PHY IP is designed to enable an alternate transmit clock to be generated with a user-defined ppm offset from the single reference clock source. This feature enables the transmitter to transit a signal that is asynchronous to the reference clock of the receiver’s CDR, providing more robust testing on the CDR of the receiver. Similar to the BERT test, the pattern generator and pattern matcher are used.

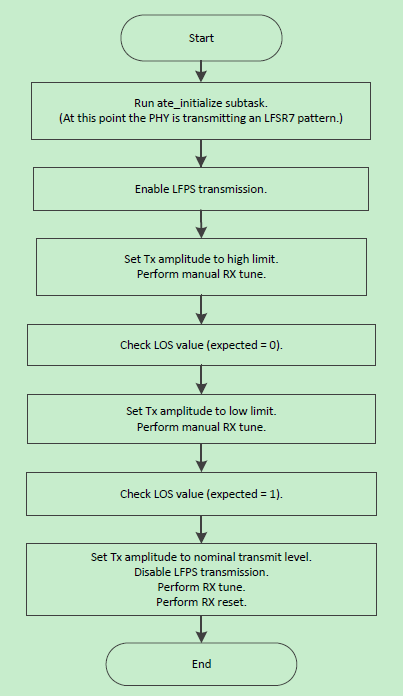


### ~~LFPS\_LOS~~

**External Loopback Required**: Y

**Wafer Sort:** N

This test sends Low Frequency Periodic Signaling (LFPS) out the transmitter and measures the Loss-of- Signal (LOS) level of the receiver. Users can set the upper and lower comparison points. When transmitting the upper voltage limit, the LOS should deassert. When transmitting the lower limit, the LOS should remain asserted.

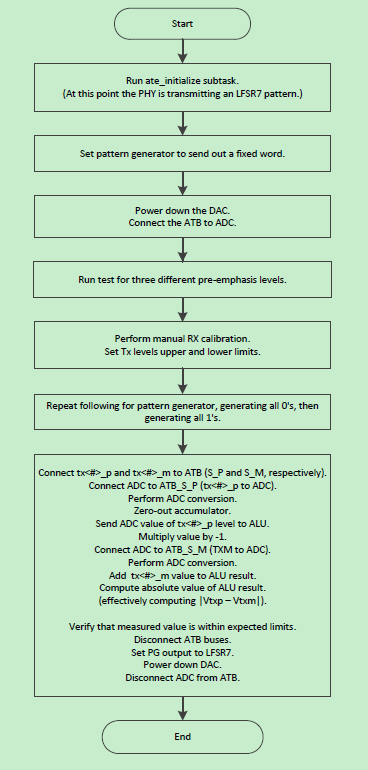


### ~~TX\_DC\_LEVELS~~

**External Loopback Required**: N

**Wafer Sort:** Y

The differential DC voltage of the PCIe 2 PHY transmitter is measured without boost, the default boost level, and a user-defined boost value. This test uses the internally available ADC to measure the voltages and compares them to user-defined limits using the ALU.



### ~~INTERNAL\_LOOPBACK~~

**External Loopback Required**: N

**Wafer Sort:** Y

This test verifies the function of the PCIe 2 PHY’s TX-to-RX digital serial loopback. This test is identical to the BERT/External Loopback test, except that the RX AFE is not exercised. An internal loopback path is exercised, bypassing the TX drivers and the RX AFE. If BERT is being run, INTERNAL\_LOOPBACK does not have to be run at board level; instead, this test can be run before packaging at wafer sort.

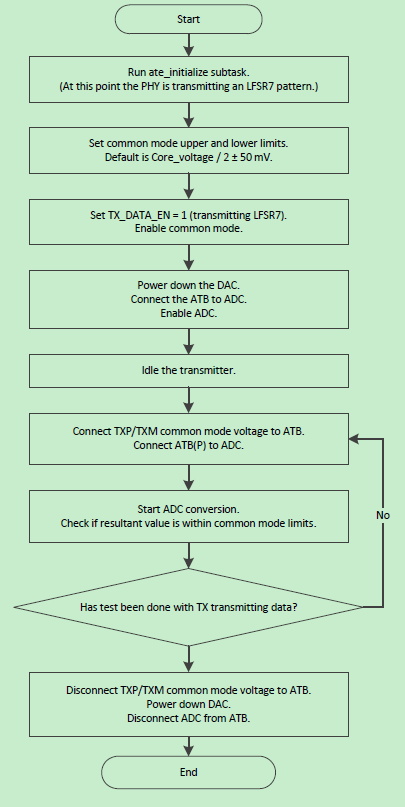
COMMON\_MODE

**External Loopback Required**: N

**Wafer Sort:** Y

**Test Plan Inclusion**: Optional

This test measures the DC transmit common-mode voltage during transmit and idle states of the PCIe 2 PHY.

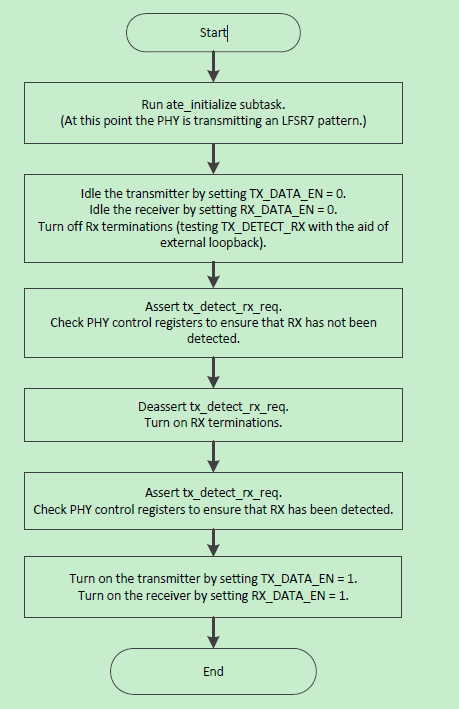


### ~~TX\_RX\_DETECT~~

**External Loopback Required**: Y

**Wafer Sort:** N

TX/RX detection is tested by turning off the PCIe 2 PHY receiver terminations and verifying that the transmitter does not detect a receiver. The receiver terminations are then enabled, and the transmitter is verified to have detected a receiver. External loopback is not required for this test; however, high-impedance DC from the transmitter is required. Therefore, the external loopback with the AC-coupling capacitors provides the high-impedance DC, because the inline capacitors are high-impedance and DC. Also note that the PCIe 2 PHY transmitter has sampling capability that is used for this test.



### ~~RX\_SCOPE\_TEST~~

**External Loopback Required**: Y

**Wafer Sort:** N

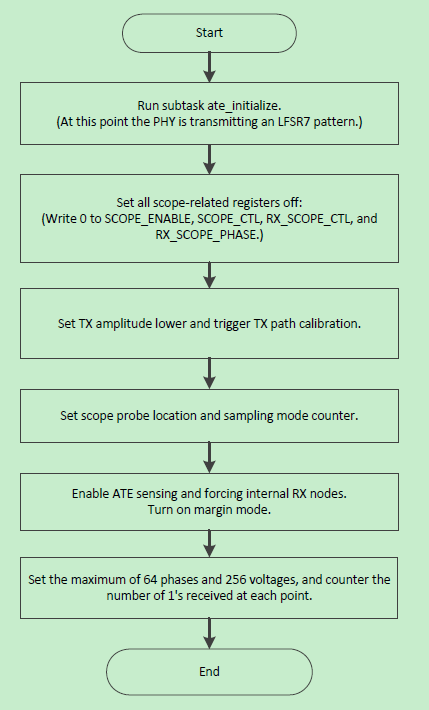
The PHY has a built-in, on-chip scope that can be used to generate a receive eye diagram.

In the ate\_rx\_scope\_test directory, the files are as follows.

■ **ate\_rx\_scope\_test.py**: Python file that generates the ATE vector Because RX\_SCOPE\_TEST requires a lot of time to generate the vector by Verilog simulation, the Python file is used to generate the ATE vector here.

■ **eye.py**: Python file that generates the eye diagram

■ **override.txt**: User parameter control for MPLL multiplier, SSC ref\_clk\_sel, TX amplitude, and JTAG clock period



## ATE Test Limits

The following table describes the recommended test limits for the ATE tests where applicable.

